IN THE CLAIMS:

Claims 1-95 (Cancelled).

96. (Currently Amended) A semiconductor device, comprising:

a first transistor having a composite gate structure containing a first conductive film, a first insulating film, and a second conductive film which overlie a first channel region and are separated therefrom by a gate dielectric layer; and

a second transistor having a single gate structure containing a third conductive film which overlies a second channel region and is separated therefrom by a gate dielectric layer;

wherein said third conductive film is comprised of a fifth conductive film over which is [[.]] disposed a sixth conductive film, said sixth conductive film and said fifth conductive film having different conductivities; and

said first conductive film has a conductivity different from the conductivity of said second conductive film.

97. (Previously Presented) The device of Claim 96, wherein said fifth and sixth conductive films are in substantial conductive contact with each other.

98. (Previously Presented) The device of Claim 96, wherein said first conductive film is disposed closer to said associated first channel region than said second conductive film.

99. (Previously Presented) The device of Claim 98, wherein said fifth conductive film has a conductivity substantially equal to the conductivity of said second conductive film.

100. (Currently Amended) The device of Claim 96, wherein said first conductive film and said fifth conductive film are fabricated at least in part from a common polysilic[[c]]on layer.

101. (Previously Presented) The device of claim 100, wherein said first conductive film and said fifth conductive film are fabricated from a common polysilicon layer and said second conductive film and said sixth conductive film are fabricated from a common polysilicon layer.

102. (Withdrawn) The device of Claim 96, wherein said fifth conductive film has a lower conductivity than said sixth conductive film.

103. (Previously Presented) The device of Claim 96, wherein at least a portion of said fifth conductive film has a conductivity substantially equal to the conductivity of at least a portion of said first conductive film.

104. (Previously Presented) The device of Claim 96, wherein said fifth conductive film has a conductivity substantially equal to the conductivity of at least a portion of said first conductive film.

105. (Previously Presented) The device of Claim 96, wherein said first and second conductive films are separated by said insulating film and said first conductive film is disposed more proximate to said associated first channel region than said second conductive film.

106. (Previously Presented) The device of Claim 96, wherein said first transistor comprises a memory transistor and said second transistor comprises a non-memory transistor.

107. (Previously Presented) The device of Claim 106, wherein said memory transistor comprises a floating gate memory cell transistor.

108. (Previously Presented) The device of claim 96, wherein said fifth and sixth conductive films are fabricated from two separate and distinct layers of material.

109. (Previously Presented) The device of Claim 106, wherein said fifth and sixth conductive films are in substantial conductive contact with each other.

110. (Previously Presented) The device of Claim 109, wherein the fifth conductive film is disposed closer to the gate dielectric layer than said sixth conductive film.

111. (Previously Presented) The device of Claim 96, wherein the fifth conductive film is disposed closer to the gate dielectric layer than said sixth conductive film.

112. (Withdrawn) A semiconductor memory device, comprising:

a memory cell transistor having a composite gate structure that overlies a memory cell transistor channel region, said associated composite gate structure including:

a trapped charge gate electrode,

a first insulating film, and

a control gate electrode separated from said trapped charge gate electrode by said first insulating film, the conductivity of said trapped charge gate electrode different from the conductivity of said control gate electrode; and

a peripheral transistor having a single gate structure that overlies a peripheral transistor channel region, said associated composite gate structure including

a gate electrode that is comprised of an upper conductive film that which is disposed over a lower conductive film, said upper conductive film and said lower conductive film having different conductivities.

113. (Withdrawn) The device of Claim 112, wherein said upper and lower conductive films are in substantial conductive contact with each other.

114. (Withdrawn) The device of Claim 112, wherein said upper conductive film has a conductivity substantially equal to the conductivity of said control gate.

115. (Withdrawn) The device of claim 112, wherein said lower conductive film and said trapped charge gate electrode are fabricated at least in part from a common polysilicon layer.

116. (Withdrawn) The device of Claim 112, wherein said lower conductive film and said trapped charge gate electrode are fabricated from a common polysilicon layer and said upper conductive film and control gate electrode are fabricated from a common polysilicon layer.

117. (Withdrawn) The device of Claim 112, wherein said upper conductive film has a higher conductivity than said lower conductive film.

118. (Withdrawn) The device of Claim 112, wherein at least a portion of said lower conductive film has a conductivity substantially equal to the conductivity of at least a portion of said trapped charge gate electrode.

119. (Withdrawn) The device of Claim 112, wherein said upper conductive film has a conductivity substantially equal to the conductivity of at least a portion of said control gate electrode.

120. (Withdrawn) The device of claim 112, wherein said upper and lower conductive films are fabricated from two separate and distinct layers of material.

121. (Withdrawn) The device of Claim 112, wherein said upper and lower conductive films are in substantial conductive contact with each other.

122. (Withdrawn) A semiconductor device, comprising:

a floating gate memory cell comprising a first transistor, the first transistor having a composite gate structure containing a first conductive film, a first insulating film, and a second conductive film which overlie a channel region and are separated from the

channel region by a gate dielectric layer, said insulating film being between the first conductive film and the second conductive film and said first conductive film being disposed more proximate to the channel region than said second conductive film; and

a second transistor comprising a non-memory transistor, the second transistor having a single gate structure containing a third conductive film which overlies a channel region and is separated therefrom by a gate dielectric layer;

wherein said third conductive film is comprised of a fifth conductive film over which is disposed a sixth conductive film, said sixth conductive film and said fifth Conductive film having different conductivities and the said fifth conductive film and said sixth conductive film being in substantial conductive contact with each other;

wherein the fifth conductive film is disposed closer to the gate dielectric layer than said sixth conductive film; and

said first conductive film has a conductivity different from the conductivity of said second conductive film.

123. (Withdrawn) The device of Claim 122, wherein said first conductive film and said fifth conductive film are fabricated at least in part from a common polysilicon layer.

124. (Withdrawn) The device of claim 123, wherein said fifth and sixth conductive films are fabricated from two separate and distinct layers of material.

125. (Withdrawn) The device of Claim 124, wherein said fifth conductive film has a lower conductivity than said sixth conductive film.

126. (Withdrawn) The device of Claim 123, wherein at least a portion of said fifth conductive film has a conductivity substantially equal to the conductivity of at least a portion of said first conductive film.

127. (Withdrawn) The device of Claim 123, wherein said fifth conductive film has a conductivity substantially equal to the conductivity of at least a portion of said first conductive film.

128. (Withdrawn) The device of claim 122, wherein said fifth and sixth conductive films are fabricated from two separate and distinct layers of material.

129. (Withdrawn) The device of Claim 128, wherein said first conductive film and said fifth conductive film are fabricated at least in part from a common polysilicon layer.

130. (Withdrawn) The device of Claim 129, wherein said fifth conductive film has a lower conductivity than said sixth conductive film.

131. (Withdrawn) The device of Claim 122, wherein said fifth conductive film has a lower conductivity than said sixth conductive film.

132. (Withdrawn) The device of claim 131, wherein said fifth and sixth conductive films are fabricated from two separate and distinct layers of material.

133. (Withdrawn) The device of Claim 132, wherein said first conductive film and said fifth conductive film are fabricated at least in part from a common polysilicon layer.

134. (New) A semiconductor device, comprising:

a memory transistor having a composite gate structure containing a first conductive film, a first insulating film, and a second conductive film that overlie a first channel region, wherein said first conductive film is disposed closer to said first channel region than said second conductive film; and

a peripheral transistor having a single gate structure containing a third conductive film and a fourth conductive film that overlie a second channel region, wherein said third conductive film is disposed closer to said second channel region than said fourth conductive film;

wherein said first conductive film and said third conductive film are fabricated from a first common polysilicon layer, and wherein an impurity concentration of said first

conductive film and an impurity concentration of said third conductive film are independent of one another.

135. (New) The semiconductor device of claim 134, wherein said second conductive film and said fourth conductive film are fabricated from a second common polysilicon layer.

136. (New) The semiconductor device of claim 135, wherein said first conductive film and said third conductive film have substantially the same thickness.

137. (New) The semiconductor device of claim 136, wherein said second conductive film and said fourth conductive film have substantially the same thickness.

138. (New) The semiconductor device of claim 137, wherein said second conductive film, said third conductive film, and said fourth conductive film have substantially the same impurity concentration.

139. (New) The semiconductor device of claim 134, wherein said second conductive film, said third conductive film, and said fourth conductive film have substantially the same impurity concentration.

140. (New) The semiconductor device of claim 138, wherein said impurity concentration of each of said second conductive film, said third conductive film, and said fourth conductive film is greater than an impurity concentration of said first conductive film.

141. (New) The semiconductor device of claim 139, wherein said impurity concentration of each of said second conductive film, said third conductive film, and said fourth conductive film is greater than an impurity concentration of said first conductive film.

142. (New) The semiconductor device of claim 140, wherein said impurity concentration of said first conductive film is between $1x10^{18}$ and $1x10^{19}$ atoms/cm^3.

143. (New) The semiconductor device of claim 142, wherein said impurity concentration of said third conductive film is between $1x10^{20}$ and $1x10^{21}$ atoms/cm^3.

144. (New) The semiconductor device of claim 143, wherein said impurity concentration of said second conductive film is between $1x10^{20}$ and $1x10^{21}$ atoms/cm^3.

145. (New) The semiconductor device of claim 144, wherein said impurity concentration of said fourth conductive film is between $1x10^{20}$ and $1x10^{21}$ atoms/cm^3.

146. (New) The semiconductor device of claim 141, wherein said impurity concentration of said first conductive film is between $1x10^{18}$ and $1x10^{19}$ atoms/cm^3.

147. (New) The semiconductor device of claim 146, wherein said impurity concentration of said third conductive film is between $1x10^{20}$ and $1x10^{21}$ atoms/cm^3.

148. (New) The semiconductor device of claim 147, wherein said impurity concentration of said second conductive film is between $1x10^{20}$ and $1x10^{21}$ atoms/cm^3.

149. (New) The semiconductor device of claim 148, wherein said impurity concentration of said fourth conductive film is between $1x10^{20}$ and $1x10^{21}$ atoms/cm^3.

150. (New) The semiconductor device of claim 134, wherein said impurity concentration of said first conductive film is between $1x10^{18}$ and $1x10^{19}$ atoms/cm^3.

151. (New) The semiconductor device of claim 150, wherein said impurity concentration of said third conductive film is between $1x10^{20}$ and $1x10^{21}$ atoms/cm^3.